IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Hanafi et al. Docket No.: BUR920040115US1

Serial No.: 10/711,450 Art Unit: 2818

Filed: September 20, 2004 Examiner: Vu, David

Title: **BURIED BIASING WELLS IN FETS (FIELD EFFECT TRANSISTORS)**

Commissioner for Patents & Trademarks
P. O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT AND RESPONSE TO RESTRICTION REQUIREMENT

In response to the Restriction Requirement mailed on August 21, 2006, Applicant hereby provisionally elects Group I, claims 1-6, drawn to a semiconductor structure, classified in class 257, subclass 376. This election is made with traverse, and Applicants hereby reserve the right to file a divisional application in connection with unelected claims 7-30, drawn to semiconductor manufacturing method, classified in class 438, subclass 175.

With regard to the Restriction Requirement, Applicants respectfully submit that the subject matter of all claims 1-30 is sufficiently related that a thorough search for the subject matter of any one group of claims would encompass a search for the subject matter of the remaining claims. Thus, Applicants respectfully submit that the search and the examination of the entire application could be made without serious burden. See MPEP § 803, in which it is stated that "if the search and examination of the entire application can be made without serious burden, the Examiner must examine it on the merits, even though it includes claims to independent or distinct inventions" (emphasis added). Applicants respectfully submit that this

policy should apply in the present application in order to avoid unnecessary delay and expense to Applicants and duplicative examination by the Patent Office.

Also, please enter the following.